N.Ex.T (NVIDIA Exceptional Talent) NCG Hiring Program

Do you have a passion for computing using new age technologies?

Do you want to work on leading-edge problems alongside some of the best & brightest in the world?

Do you like working in a dynamic working environment that involves creative problem solving and thinking on your feet?

We, at NVIDIA, want to find and bring the brightest young technologists of our generation to do their life's best work at NVIDIA.

We are hiring across multiple positions in our HW teams and a brief about the teams and their requirements is given below

GPU ARCHITECTURE TEAM

GPU architecture team is engaged in the development of industry leading high performance and power efficient GPUs.
Specific areas include architecture modeling, analysis and performance verification. The team works on GPUs across all application domains such as gaming for PC and mobile devices, professional graphics & visualization and high-performance computation.
Skills you will use/develop:

- C++ modeling, test development
- RTL design, debug
- ASIC design & verification tools, methodologies
- Computer architecture, Graphics, GPU micro-architecture, parallel computing
- Performance evaluation, analysis and debug
- Perl/Python scripting

Areas you will be working on:
COMPUTER ARCHITECTURE; MEMORY SYSTEMS ARCHITECTURE, COMPILER ARCHITECTURE/ PERFORMANCE MODELING

GPU ASIC DESIGN / VERIFICATION TEAM

Today NVIDIA's GPUs simulate human intelligence, running deep learning algorithms and acting as the brain of super computers, robots, and self-driving cars that can perceive and understand the world We are seeking a passionate, innovative, and highly motivated senior verification engineer to join us in the development of the next generation of PCI Express controllers used in NVIDIA's GPUs and SOCs In this position, you will be responsible for verification of the ASIC design, architecture and micro architecture using advanced verification methodologies You are expected to understand the design and implementation, define the verification scope, develop the verification infrastructure and verify the correctness of the design You will be working with architects, designers, pre and post silicon verification teams to accomplish your tasks
What you'll be doing

- Develop test plans, tests and verification infrastructure for PCIE at IP/sub system/SOC level
- Create verification environment using UVM methodology
- Create reusable bus functional models, monitors, checkers and scoreboards
- Drive functional coverage driven verification closure
- Work with architects, designers and post silicon teams

Ways to stand out from the crowd

- Good knowledge of PCIE protocol Gen 3 and above
- Good debugging and problem-solving skills
- Good communication skills and ability desire to work as a team player

TEGRA SOC DESIGN & VERIFICATION

Tegra ASIC team (Design Verification)

As a Hardware Engineer at NVIDIA you will design and implement the industry's leading Graphics, Video and Mobile Communications Processors. Specific areas include 2D and 3D graphics, mpeg, video, audio, network protocols, high-speed IO interfaces and bus protocols, and memory subsystem design. You will be responsible for Architecture and micro-architecture design of the ASICs, RTL design and synthesis, Logic and Timing verification using leading edge CAD tools and Semiconductor process technologies

Areas you will be working on:

- ASIC, RTL, DESIGN AND VERIFICATION OF PROCESSORS
- Low Power verification
- Power Estimation and Modeling
- PCIe Design verification
- Functional / Formal verification

CPU VERIFICATION TEAM

As a design verification engineer in the Nvidia's CPU team, you will be working on the next generation of 64bit ARM architecture-based CPUs and SOCs. As part of this assignment, the intern will get a chance to learn about computer architecture at a very granular level, System Verilog, Unit/Cluster /SOC Verification, cutting edge verification methodologies and C/C++/ASM programming. The intern also will get an opportunity to get familiar with industry standard tools in verification and validation. During the course of the internship, the intern will contribute to building test benches, developing architectural simulators, modifying random instruction generators and creating stimulus for verification and validation of different units of the CPU and SOC.

Areas you will be working on

- Computer Architecture
- Digital Design and Programming in C/C++/Perl
- ARM, CPU Design and Verification/ Validation

ASIC-PD (Timing Closure / VLSI)

VLSI team works in the areas of RTL Design, Verification, Design for Test, CAD tools, Synthesis, Timing, Place & Route, Circuit Design, Silicon Bring-up and Characterization. Responsible for state-of-the-art methodologies, tools, flows and project execution on all Nvidia GPU, CPU, Auto, and Switch chips. As a team member you will be working on one or more such areas.

Skills you will use/develop:

- RTL Design, VCS, SV, UVM, Formal
- Verilog, C/C++, Python, TCL, Perl
- Logic Scan Test, Memory Test, High-speed IO Test, In-System Test
- Synthesis, Timing Closure (Primetime)
- Physical Design, Innovus, ICC2, Physical extraction, Place and Route, Floorplan
- SRAM, Analog, Digital circuit design, Hspice, EMIR, Silicon Correlation (ATPG, data visualization & analysis)
- Layout (Cadence Virtuoso)
- Silicon characterization for ageing, DPPM, Signal Integrity, Power Integrity, and familiarity with PC/SOC sub-system Architecture

INFRASTRUCTURE TOOLS DEVELOPMENT (Trace Tools / Graphics)

A key part of NVIDIA’s strength is our unique tools for analysis, visualization, debug and automated regressions. We are looking for bright engineers to participate in our fast-paced Agile software

team and to continue and improve our extremely high production quality standards. These tools are used by all the engineers in NVIDIA.
We are continuously pushing the envelope and needing the next generation of tools to enable the next generation of chips. The tools we build involve high compute infrastructure to allow very large scale distributed, cross-platform runs of mission critical proprietary applications, creating integrated development and debugging environments (such as Eclipse), implementing software engineering methodologies and tools to improve code quality, creating and driving quality build and release processes, and driving the performance improvement of chips we develop

Areas you will be working on

- Object-oriented programming and design background: Object Oriented Perl, C++ or Java preferred
- Interpreted language skills – Object Oriented Perl preferred
- Experience in software development life cycle in Linux based platforms preferred